operation of the counter which accidentally happens to instantaneously yield the correct initial, all high condition. However, the latch 14a will not reactivate because it has been latched to its deactive (no reset) state.

Referring to Figures 3a through 3c, the power supply signal Vcc shown in Figure 3a ramps up at 22 (when turned on) to a Vcc level 24. During the ramping (at 22), as shown in Figure 3b, the pulse generator 16 signal undergoes the transition to the high level 26 causing the functional block logic to go to "ready" (S=1), as indicated at 30 in Figure 3c. When the pulse generator 16 signal is high (Figure 3b) the logic AND is high (Figure 3c), the pulse generator 16 signal goes low (R=0) as indicated at 28 in Figure 3b. The pulse generator 16 signal being low causes the reset signal to go low releasing the logic in the functional block F, as indicated at 32 in Figure 3c. Logic glitches, indicated at 34 and 36, do not reactivate the reset signal, in one embodiment of the present invention, due to the latching action.

In the event that the I_0 through I_N AND signals indicate a high prior to the pulse generator 16 signal high 26, as indicated in Figures 4b and 4c, the circuit 10 still functions correctly in one embodiment. For example, as shown in Figure 4a, during the ramp indicated at 22, the pulse generator 16 signal goes high as indicated at 26 in

Figure 4b. Since the pulse generator 16 signal is high and the logic AND is high, the pulse generator 16 signal goes low as indicated at 28. The reset low results, causing the logic to release. Again logic glitches indicated at 34 and 36 do not reactivate the reset signal.

The use of the latch 14 may be advantageous in some embodiments since it is useful for noise protection in low voltage applications. Noise on the supply or noise coupled from other lines may cause bouncing on critical nodes. This bouncing may trigger the next stage to unexpectedly change state.

The functional blocks may be comprised of dynamic or static logic. In addition, the functional block may be a phase-locked loop (PLL). By allowing dynamic logic, the state of the blocks that are used for normal operation may be monitored. Once they operate normally (reset is gone), they do not retrigger the reset pulse because of the latching operation.

Referring to Figure 5, in accordance with one embodiment of the present invention, a particular pulse generator 16 is described. However, the present invention is in no way limited to the particular design depicted in Figure 5. A variety of pulse generator 16 designs may be utilized in the embodiments shown in Figures 1 and 2.

The pulse generator 16 shown in Figure 5 includes activation circuits 40 that handle the feedback of the

output pulse from pulse generator 16 along the line 55. In particular, the activation circuits 40 receive the feedback of the output pulse so that, once the pulse generator 16 signal goes away, the pulse generator 16 is not inadvertently reactivated. The activation circuits 40 may also ensure that a predetermined supply voltage level is achieved before beginning the power-on reset pulse generator 16 operation in one embodiment.

The activation circuits 40 provide outputs 53a and 53b to the capacitor circuits 44. A variety of known capacitor circuits 44 may be utilized in some embodiments of the present invention. One capacitor circuit 44, shown in Figure 6, receives the supply voltage Vcc at the node 53a through the capacitor 56. The Vcc-connected capacitor 56 is pulled to Vcc. A capacitor 64, coupled to Vss (or ground), remains at ground initially.

The capacitor 56 slowly discharges to ground through the transistor 58 that acts as a current source. Meanwhile, the capacitor 64 begins to charge up to Vcc through the low current transistor 60 and the pass gate transistor 62. Therefore, the capacitor circuits 44 count on the current to charge up or down each capacitor 56 or 64 above the trip point of the ensuing hysteresis sense stages 48. In addition, the capacitor 64, charging towards Vcc, depends on the capacitor 56 that is charging to ground